In the claims:

Please replace all previous versions of the claims with the following:

1. (Currently amended): A semiconductor device comprising:
a common substrate;
an SRAM device implemented on the common substrate and isolated by a first isolation technique; and
a flash EPROM device implemented on the common substrate and isolated by a second isolation technique,
wherein the first isolation technique and the second isolation technique are different and implemented non-concurrently ~~sequentially~~.

2. (Original): The semiconductor device according to claim 1 wherein the first isolation technique is an STI technique.

3. (Original): The semiconductor device according to claim 1 wherein the second isolation technique is a LOCOS isolation technique.

4. (Original): The semiconductor device according to claim 1 wherein the SRAM device is coupled to the flash EPROM device for transmitting signals between the SRAM device and the flash EPROM device.

5. (Currently amended): A system containing for allowing different types of isolation techniques during fabrication of a semiconductor device, comprising:

a common substrate having a first portion on which a first isolation technique is implemented during processing and a second portion on which a second isolation technique is implemented during processing, wherein the first isolation technique and the second isolation technique are different and implemented non-concurrently ~~sequentially~~;

an SRAM device implemented on the first portion of the substrate; and

a flash EPROM device implemented on the second portion of the substrate.

6. (Original): The system according to claim 5 wherein the SRAM device is coupled to the flash EPROM device for transmitting signals between the SRAM device and the flash EPROM device.

7. (Original): The system according to claim 5 wherein the first isolation technique is an STI technique.

8. (Original): The system according to claim 5 wherein the second isolation technique is a LOCOS technique.

9. (Currently amended): A semiconductor device comprising:

a common substrate having a first portion on which an STI isolation technique is implemented during processing and a second portion on which a LOCOS isolation technique is implemented during processing, wherein the STI isolation technique and the LOCOS isolation technique are implemented non-concurrently ~~sequentially~~;

an SRAM device implemented on the first portion of the substrate; and

a flash EPROM device implemented on the second portion of the substrate.

10. (Original): The semiconductor device according to claim 9 wherein the SRAM device is coupled to the flash EPROM device for transmitting signals between the SRAM device and the flash EPROM device.

11-17. (Previously canceled).

18. (Currently amended): A semiconductor device, comprising:

a common substrate;

a first region formed on the common substrate, the first region comprising an SRAM device, a first active region, and a first isolation region having a first isolation structure formed of a first material, the SRAM device overlying the first active region, the first active region isolated by the first isolation structure ~~region, the first active region and the first isolation region forming a uniform region made of a first material~~; and

a second region formed on the common substrate, the second region comprising a flash EPROM device, a second active region, and a second isolation region having a second isolation structure formed of a second material, the flash EPROM device overlying the second active region, the second active region isolated by the second isolation structure ~~region, the second active region and the second isolation region forming a uniform region made of a second material~~,

wherein the first isolation structure is contiguous to and different from the second isolation structure.

19. (Previously added): The semiconductor device of claim 18, wherein the first isolation structure is a shallow trench.

20. (Previously added): The semiconductor device of claim 18, wherein the second isolation structure is a LOCOS isolation structure.

21. (Previously added): The semiconductor device of claim 18, wherein the first material comprises an insulating oxide.

22. (Previously added): The semiconductor device of claim 18, wherein the second material comprises an insulating oxide.

23. (New): A semiconductor device comprising:

a common substrate;

an SRAM device implemented on the common substrate and formed over a first active region on a first isolated structure; and

a flash EPROM device implemented on the common substrate and formed over a second active region on a second isolated structure, the second isolated structure having a first portion extending a first depth into the substrate and a second portion containing the second active region and extending a second depth into the substrate, the first depth larger than the second depth,

wherein the first isolated structure and the second isolated structure are different.

24. (New): The semiconductor device of claim 23, wherein the first isolated structure and the second isolated structure are contiguous.

25. (New): The semiconductor device of claim 23, wherein the first isolated structure and the second isolated structure both comprise an oxide material.

26. (New): A system containing a semiconductor device having a plurality of isolated structures, the system comprising:

a common substrate having a first portion on which a first isolation technique is implemented during processing and a second portion on which a second isolation technique is implemented during processing, the second portion having a first segment extending a first depth into the substrate and a second segment containing an active region extending a second depth into the substrate, wherein the first depth is larger than the second depth and further wherein the first isolation technique and the second isolation technique are different;

an SRAM device implemented on the first portion of the substrate; and

a flash EPROM device implemented on the second portion of the substrate.

27. (New): The system of claim 26, wherein the first portion and the second portion are contiguous.

28. (New): The system of claim 27, wherein the first portion and the second portion both comprise an oxide material.